

entity Fsm: Fsm

850

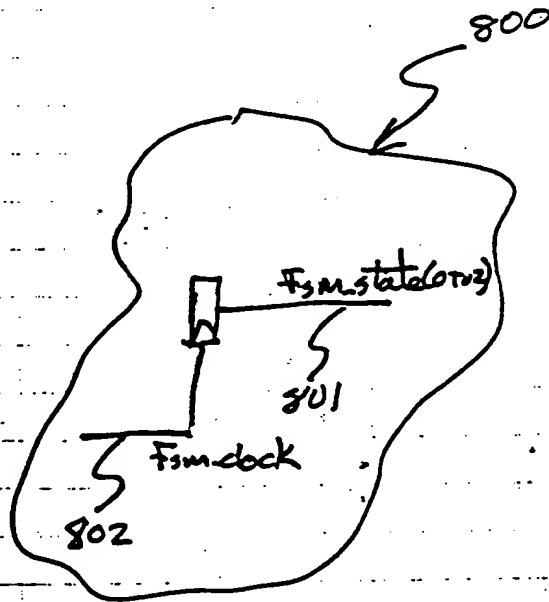


FIG. 8B (Amended)
(Prior Art)

entity Fsm IS

PORT(
.... ports for entity Fsm....

);

ARCHITECTURE Fsm OF Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity...

fsm-state(0 to 2) <= ... signal 801....

```
853 E  --!! Embedded Fsm : exampleFsm;
859 E  --!! clock       : (fsm_clock);
854 E  --!! state_vector : (fsm_state(0 to 2));
855 E  --!! states       : (s0, s1, s2, s3, s4);
856 E  --!! state_encoding : ('000', '001', '010', '011', '100');
857 E  --!! arcs         : (s0 => s0, s0 => s1, s0 => s2,
                        s1 => s2, s1 => s3, s2 => s2,
                        s2 => s3, s3 => s4, s4 => s0);
858 E  --!! end Fsm;
```

852

END;

FIG. 8C (Amended)